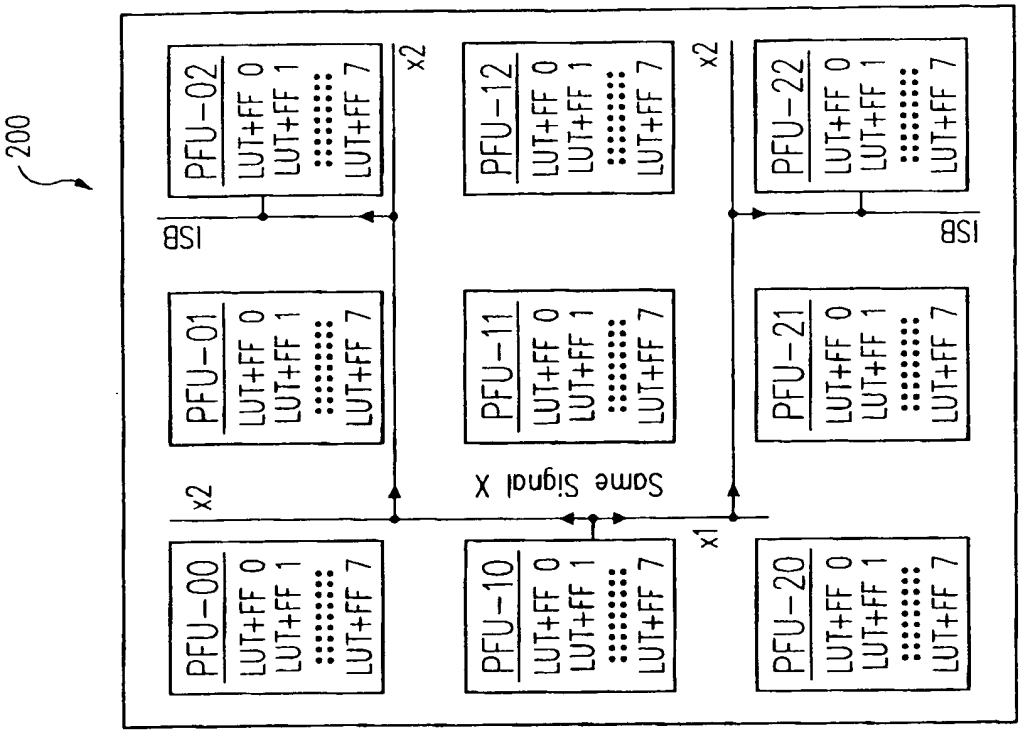
200
PFU-00
PFU-01
PFU-02
PFU-10
PFU-11
PFU-12
PFU-20
PFU-21
PFU-22
LUT+FF 0
LUT+FF 1
LUT+FF 7
ISB
x2
x1
Some Signal X

FIG. 2

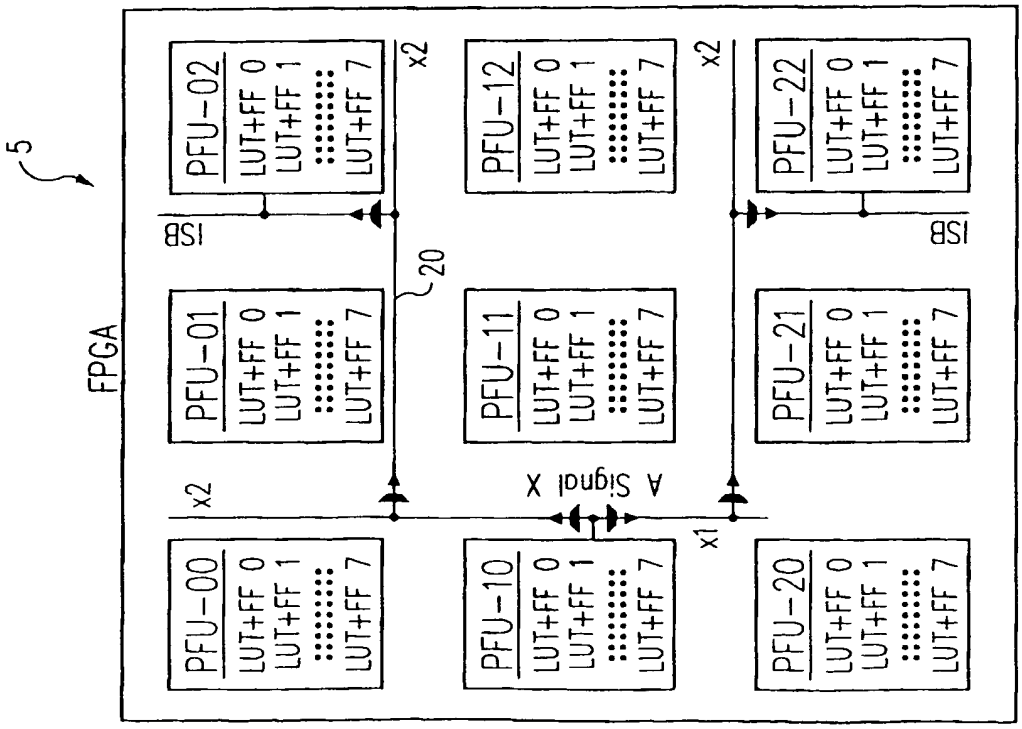
5
FPGA
PFU-00
PFU-01
PFU-02
PFU-10
PFU-11
PFU-12
PFU-20
PFU-21
PFU-22
LUT+FF 0
LUT+FF 1
LUT+FF 7
ISB
x2
x1
20
A Signal X

FIG. 1

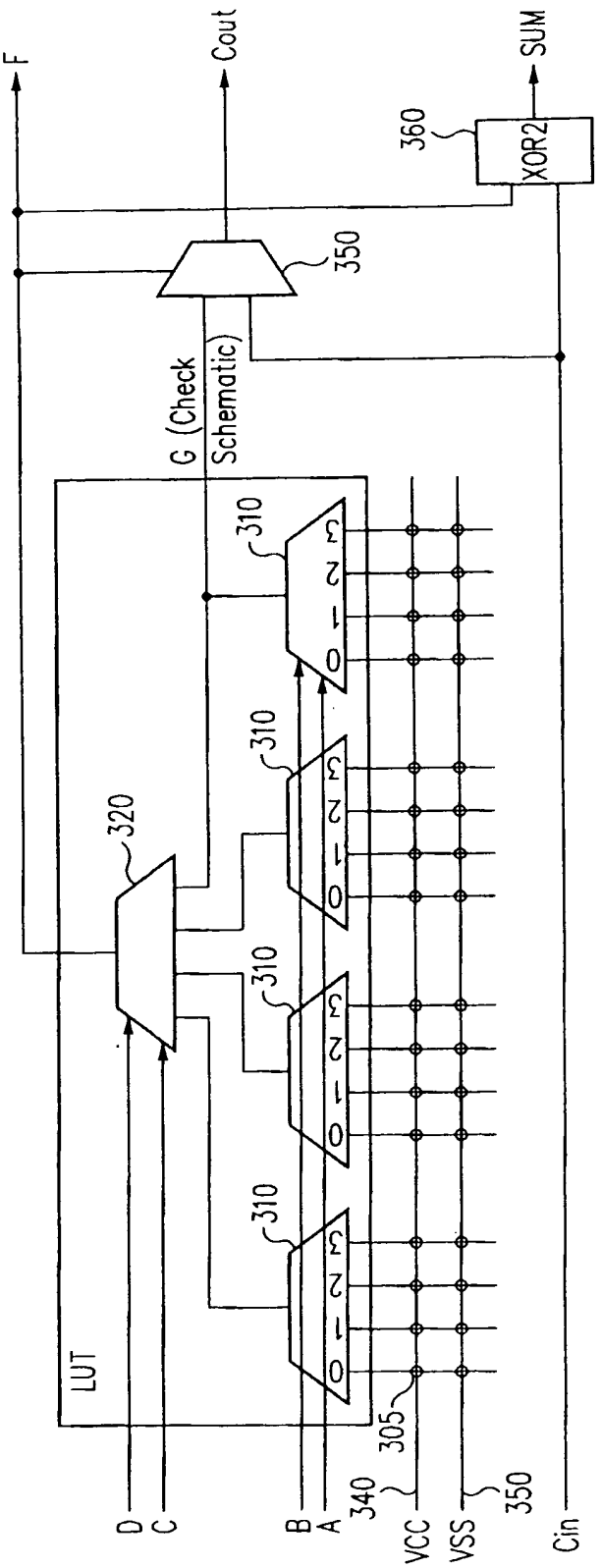
F
Cout
SUM
360
XOR2
350
G (Check Schematic)
310
320
LUT
D
C
B
A
340
305
VCC
VSS
350
Cin

FIG. 3

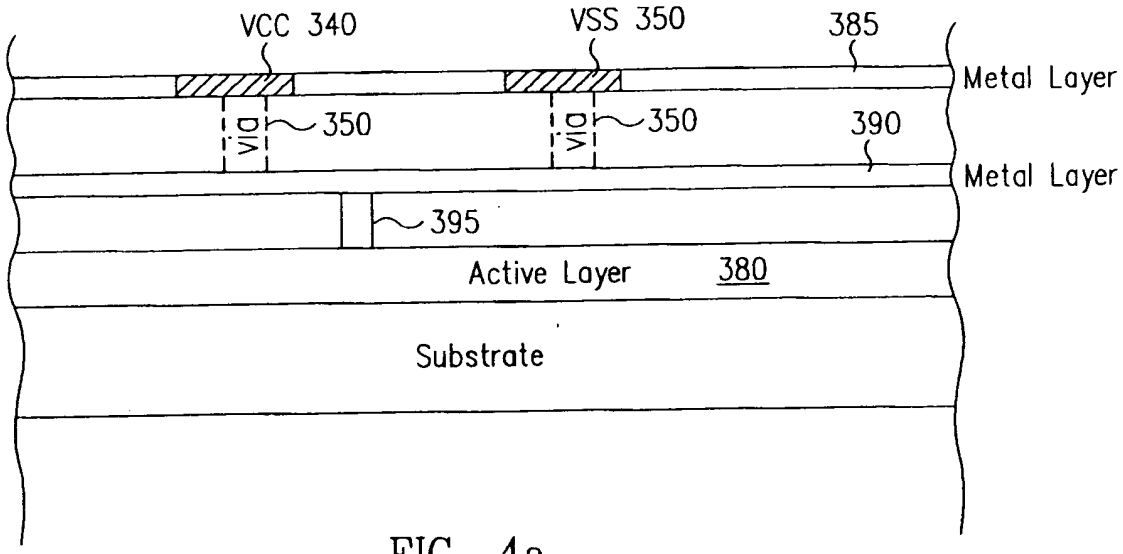
VCC 340
VSS 350
385
Metal Layer
via
350
via
350
390
Metal Layer
395
Active Layer 380
Substrate

FIG. 4a

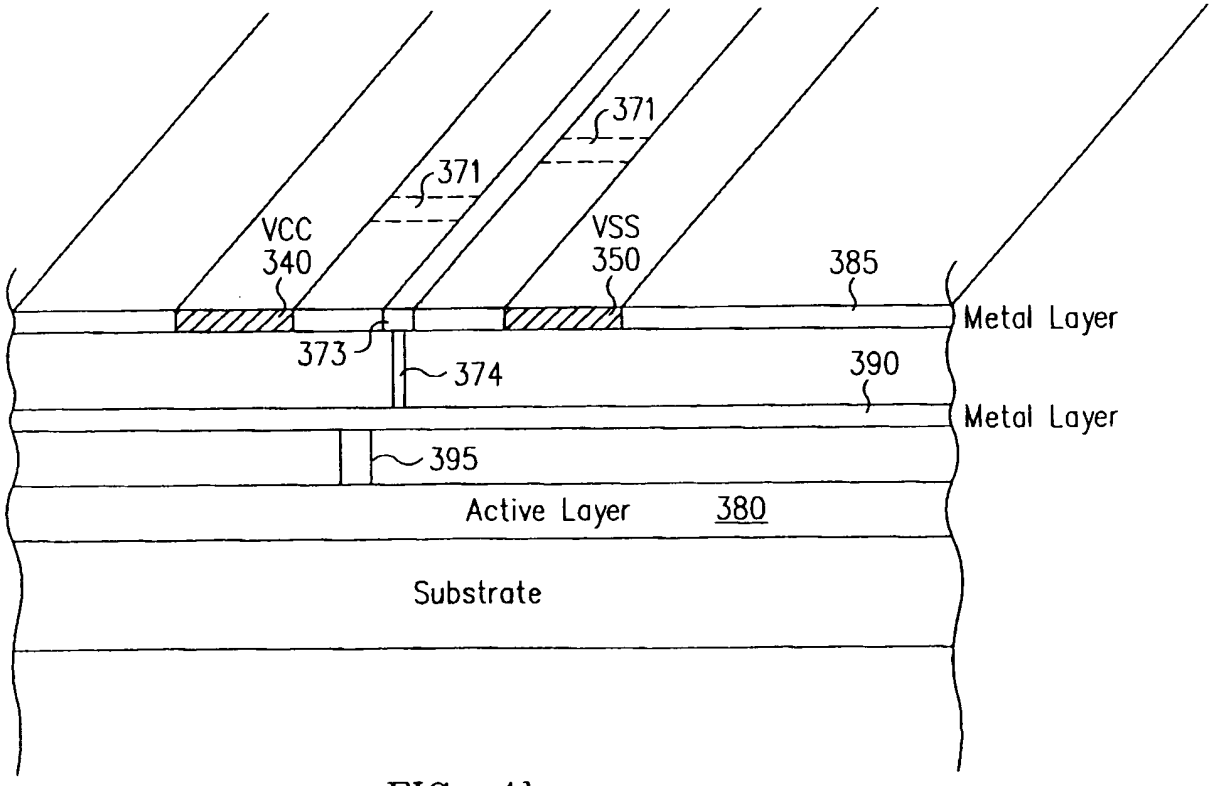
371
371
VCC
340
VSS
350
385
Metal Layer
373
374
390
Metal Layer
395
Active Layer 380
Substrate

FIG. 4b

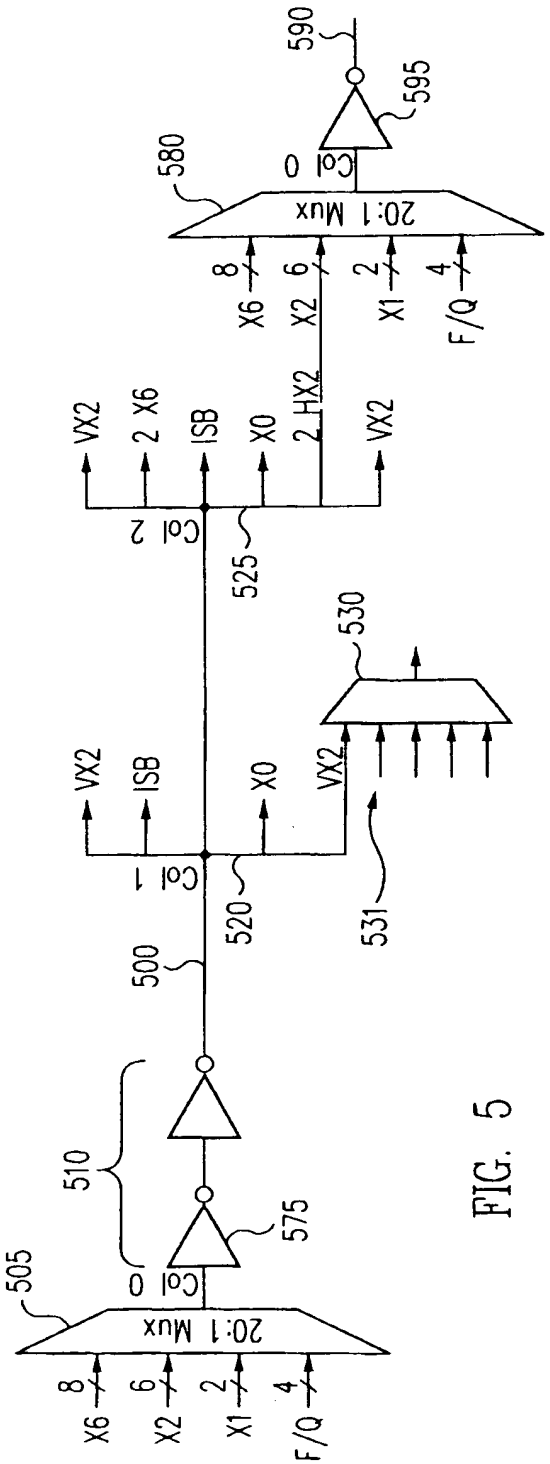
505
20:1 Mux
Col 0
575
510
500
Col 1
520
531
530
525
Col 2
580
20:1 Mux
Col 0
595
590
X6
X2
X1
F/Q
VX2
ISB
X0
2 HX2
2 X6

FIG. 5

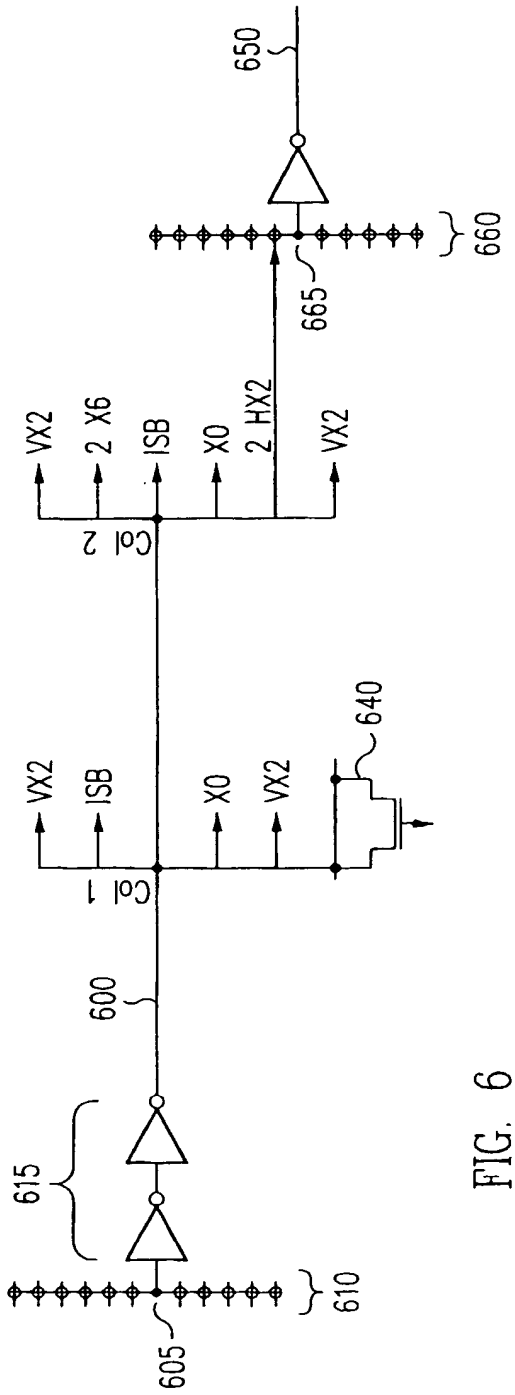
605
610
615
600
Col 1
640
Col 2
665
660
650
VX2
ISB
X0
2 HX2
2 X6

FIG. 6

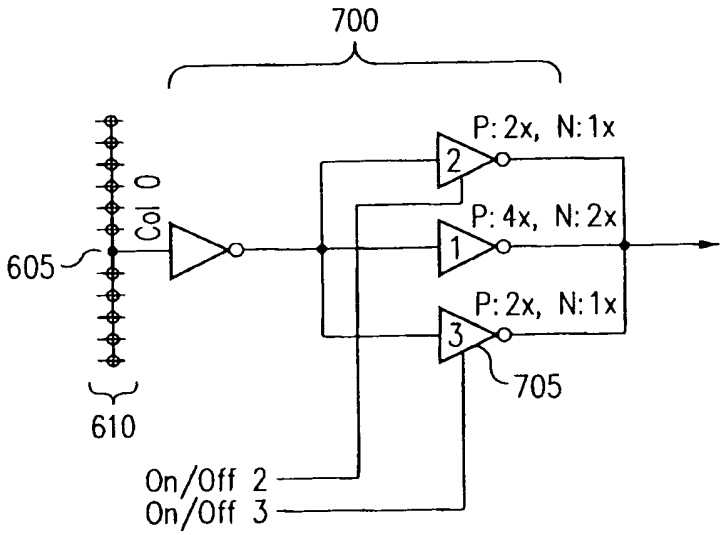

FIG. 7